Notice of Allowability	Application No.	Applicant(s)	
	10/759,072	ONOZAWA ET AL.	
	Examiner	Art Unit	
	Angela M. Lie	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/13/2005*.

2. ☒ The allowed claim(s) is/are *3-11,13-21,23-36,38-42 and 47-51*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Wilson Lee

WILSON LEE
PRIMARY EXAMINER

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the claim 50, in line 11, insert --one-- after phrase "recited in any" and before "of".

In claim 51, in line 10, insert --one-- after phrase "recited in any" and before "of claims".

The Examiner's amendment has been made to correct minor typographical errors.

Reasons for Allowance

1. Claims 3-11, 13-21, 23-36, 38-42 and 47-51 are allowed.

2. The following is an examiner's statement of reasons for allowance:

As to claim 4, the prior art fails to teach a capacitive load driving circuit, comprising: an input terminal, a rising edge delay circuit, a falling edge delay circuit, an amplifying circuit, an output switch device, wherein those elements are connected in the

manner as disclosed in claim 4, and wherein the rising edge delay circuit comprises a capacitive element and a parallel circuit of resistive element and a switch element.

As to claims 3 and 5-7, those claims are allowed by the virtue of their dependency on claim 4.

As to claim 8, the prior art fails to teach a capacitive load driving circuit, comprising: an input terminal, a rising edge delay circuit, a falling edge delay circuit, an amplifying circuit, an output switch device, wherein those elements are connected in the manner as disclosed in claim 8, and wherein the falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element.

As to claims 9-11, those claims are allowed by the virtue of their dependency on claim 8.

As to claim 14, the prior art fails to teach a capacitive load driving circuit, comprising: an input terminal, a falling edge delay circuit, a rising edge delay circuit, an amplifying circuit, an output switch device, wherein those elements are connected in the manner as disclosed in claim 14, and wherein the rising edge delay circuit comprises capacitive element and a parallel circuit of a resistive element and a switch element.

As to claims 13 and 15-17, those claims are allowed by the virtue of their dependency on claim 14.

As to claim 18, the prior art fails to teach a capacitive load driving circuit, comprising: an input terminal, a falling edge delay circuit, a rising edge delay circuit, an amplifying circuit, an output switch device, wherein those elements are connected in the

manner as disclosed in claim 18, and wherein the falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element.

As to claims 19-21, those claims are allowed by the virtue of their dependency on claim 18.

As to claim 23, the prior art fails to teach a capacitive load driving circuit, comprising: an input terminal, a front edge delay circuit, a back edge delay circuit, an amplifying circuit, an output switch device, wherein those elements are connected in the manner as disclosed in claim 23, and wherein the front edge delay comprises a first capacitive element and a first series circuit having a first resistive element and a first switch element, the back edge delay circuit comprises a second capacitive element and a second series circuit having a second resistive element and a second switch element, and the first series circuit and the second series circuit are connected in parallel.

As to claims 24-26, those claims are allowed by the virtue of their dependency on claim 23.

As to claim 27, the prior art fails to teach a capacitive load driving circuit, comprising: an input terminal, a front edge delay circuit, a back edge delay circuit, an amplifying circuit, an output switch device, wherein those elements are connected in the manner as disclosed in claim 27, and wherein the front-edge delay circuit comprises a first resistive element and a first capacitive element, the back-edge delay circuit comprises a second capacitive element and a series circuit having a second resistive element and a switch element, and the first resistive element and the series circuit are connected in parallel.

As to claims 28-31, those claims are allowed by the virtue of their dependency on claim 27.

As to claim 32, the prior art fails to disclose a capacitive load driving circuit comprising: an input terminal, a front edge delay circuit, a back edge delay circuit, an amplifying circuit, an output switch wherein those elements are connected in the manner as disclosed in claim 32, and wherein a delay time of the front edge is adjusted by varying a count value of the first counter and a delay time of the back edge is adjusted by varying a count value of the second counter.

As to claim 33, this claim is allowed by the virtue of its dependency on claim 32.

As to claim 34, the prior art fails to teach a capacitive load driving circuit comprising: an input terminal, a front edge delay circuit, a back-edge delay circuit, an amplifying circuit, an output switch device, wherein those elements are connected in the manner as disclosed in claim 34, and wherein a first output switch device in the first capacitive load driving circuit is connected between a power line and a capacitive load; and a second output switch device is the second capacitive load driving circuit connected between the capacitive load and a reference voltage.

As to claims 35 and 36, those claims are allowed by the virtue of their dependency on claim 34.

As to claim 38, the prior art fails to disclose a capacitive load driving circuit comprising: an input terminal, a front edge delay circuit, a pulse width adjusting circuit comprising a monostable multivibrator, an amplifying circuit, and an output switch

device, wherein all those elements are connected in the manner as disclosed in claim 38.

As to claims 39-41, those claims are allowed by the virtue of their dependency on claim 38.

As to claim 42, the prior art fails to teach a capacitive load driving circuit, comprising: a front edge delay circuit, a pulse width adjusting circuit, a first counter, a second counter, an amplifying circuit and an output switching device wherein all those elements are connected in the manner as disclosed in claim 42.

As to claim 47, the prior art fails to disclose a capacitive load driving circuit comprising: a first and a second capacitive load driving circuits, an input terminal, a front-edge delay circuit delaying circuit, a pulse width adjusting circuit, an amplifying circuit, an output switching device wherein all those elements are connected in the manner as disclosed in claim 47, and wherein a first output switch device in the first capacitive load driving circuit is connected between a power line and a capacitive load; and a second output switch device in the second capacitive load driving circuit is connected between the capacitive load and a reference voltage.

As to claims 48 and 49, those claims are allowed by the virtue of their dependency on claim 47.

As to claims 50 and 51, those claims are allowed by at least comprising an allowed subject matter shown in claims 4, 8, 14, 18, 23, 27, 32, 34, 38, 42 or 47.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

The Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 6329980 discloses a driving circuit for display device
- US 5541452 discloses an image device and its driving circuit
- US 20020054001 discloses a driving method and driving circuit of plasma display panel
- US 5311169 discloses a method and apparatus for driving capacitive display device.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angela M. Lie whose telephone number is 571-272-8445. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Angela M Lie

WILSON LEE
PRIMARY EXAMINER